UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte JOHN S. KRESGE, ROBERT D. SEBESTA, DAVID B. STONE and JAMES R. WILCOX

Appeal No. 2005-1715
Application No. 10/040,745

ON BRIEF

Before McQUADE, NASE, and BAHR, Administrative Patent Judges.

NASE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 80 to 97, which are all of the claims pending in this application.

We AFFIRM-IN-PART.

BACKGROUND

The appellants' invention relates, in general, to an electronic package for mounting of integrated circuits, and in particular, to an organic multi-layered interconnect structure for use in such a package (specification, p. 1). A copy of the claims under appeal is set forth in the appendix to the appellants' brief.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Peterson et al. (Peterson)	4,882,454	Nov. 21, 1989
Frankeny et al. (Frankeny)	5,691,041	Nov. 25, 1997

Claims 80, 82 to 87, 91 and 93 to 97 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Peterson.

Claims 81, 88 and 92 stand rejected under 35 U.S.C. § 103 as being unpatentable over Peterson.

Claims 89 and 90 stand rejected under 35 U.S.C. § 103 as being unpatentable over Peterson in view of Frankeny.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejections, we make reference to the answer (mailed December 16, 2003) for the examiner's complete reasoning in support of the rejections, and to the brief (filed September 23, 2003) and reply brief (filed February 4, 2004) for the appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the examiner. As a consequence of our review, we make the determinations which follow.

The anticipation rejection

We sustain the rejection of claims 80, 82 to 86, 91 and 93 to 97 under 35 U.S.C. § 102(b) as being anticipated by Peterson but not the rejection of claim 87.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal Bros. Inc. v. Union Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir.), cert. denied, 484 U.S. 827 (1987). The inquiry as to whether a reference

anticipates a claim must focus on what subject matter is encompassed by the claim and what subject matter is described by the reference. As set forth by the court in Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 (1984), it is only necessary for the claims to "'read on' something disclosed in the reference, i.e., all limitations of the claim are found in the reference, or 'fully met' by it."

Claims 80, 87 and 91 read as follows:

80. A method of making a multi-layered interconnect structure adapted for electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections, said method comprising the steps of:

providing a thermally conductive layer including first and second opposing surfaces;

positioning first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively; and

positioning first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate, respectively, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate.

87 . A method of making an electronic package comprising the steps of:

providing a semiconductor chip having a first surface including a plurality of contact sites thereon;

providing a multi-layered interconnect structure adapted for electrically interconnecting said semiconductor chip to a circuitized substrate, said

multi-layered interconnect structure including a thermally conductive layer, having first and second opposing surfaces, first and second dielectric layers positioned on said first and second opposing surfaces, respectively, and first and second pluralities of electrically conductive members positioned on said first and second dielectric layers, respectively;

providing a first plurality of solder connections on said first plurality of electrically conductive members; and

connecting respective ones of said first plurality of solder connections to respective ones of said plurality of contact sites on said semiconductor chip, said thermally conductive layer being composed of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip.

91. A method of making a multi-layered interconnect structure adapted for electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections, said method comprising the steps of:

providing a thermally conductive layer including first and second opposing surfaces;

positioning first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively;

positioning a first electrically conductive layer within said first dielectric layer;

positioning a second electrically conductive layer between said first electrically conductive layer and said thermally conductive layer wherein said second electrically conductive layer comprises a first plurality of shielded signal conductors; and

positioning first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate, respectively, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate.

Peterson's invention is directed to a printed wiring board having a core surrounded by multiple layers of dielectric and conductive materials optimized for their thermal expansion qualities. Peterson teaches (column 1, lines 14-43) that:

> To relieve the leaded-package limitations, the industry has developed surface mount technology for IC packaging. This in turn has caused several problems for the printed wiring board. The first of these problems is increased heat that must be dissipated. Since the density of components has increased, then there is more thermal energy generated in a given surface area than there was using leaded technology. Therefore, the printed wiring board should provide some means for transporting the additional heat flux.
>
> It is an object of the invention to provide a printed wiring board that functions as a heat-sink.
>
> It is also an object of the invention to provide a structure allowing good thermal conductivity from an internal thermal plane to the exterior of the printed wiring board for removal of heat.
>
> Another heat related problem is that of the difference in thermal coefficients between the components and the printed wiring board. The heat will cause both the individual components and the printed wiring board to expand. As there is a high probability that there is a difference in the rate of expansion. Therebetween, the solder joint between the component and the printed wiring board will be stressed. Also, deflection of the printed wiring board will produce stress in the solder joints.
>
> It is therefore an object of the invention to have a printed wiring board structure that possesses similar thermal expansion characteristics to surface mount components to be attached.

Figure 1 of Peterson illustrates a cross-section of a portion of the finished printed wiring board. The core section 102 is surrounded by alternating layers of conductive

material 105 and dielectric material 101. This cross-section also shows two device mounting pads 103 and 104 for soldering surface-mount devices. The device mounting pads 103 and 104 are electrically interconnected by blind-plated vias such as 106 and 107 interconnecting through the conducting layers 105 and the core 102 by way of the blind plated hole 108.

Peterson's surface mounting pads 103 and 104 are elongated where the surface mount devices are to be attached. There are two major reasons for this. The first purpose is to allow a greater surface area to solder each surface mount device. The second purpose is more important. The elongated pads 103 and 104 along with the underlying vias 106 and 107 allow a spring action to be used to help absorb any difference in thermal expansion between the printed wiring board and the surface mount devices. This greatly reduces the stress that is placed on the soldered connection and thus promotes reliability. Because the dielectric and restraining layers 101 can, in some embodiments of the invention, be somewhat pliable, the blind-plated vias 106 and 107 may be allowed to flex. This further increases the spring action for the mounting pads 103 and 104.

Peterson's core section 102 may be made of copper, copper clad invar, copper clad molybdenum, aluminum, or other suitable materials. This core not only adds

structural rigidity to the finished board, but it also functions as a heat sink and as a tooling plate during construction. The dielectric materials chosen may include aramid fibers, a glass fabric, quartz fabric or other suitable material. In one preferred embodiment of the invention, the conducting layers 105 are composed of copper.

Peterson teaches (column 2, lines 40-49) that:

> The ratio between the high expansion metal and dielectric and the low expansion rate core may be adjusted to allow a controlled CTE (coefficient of thermal expansion) circuit board to be fabricated for use with surface mount devices. Ideal performance in a surface mount application is achieved when CTE, thermal, weight and electrical properties are optimized by proper choice of materials and geometries. Core modifications can also be made to enhance thermal, CTE or weight properties when specific needs must be met.

Claim 87

Claim 87 is not anticipated by Peterson. Peterson does not teach connecting respective ones of the first plurality of solder connections of the multi-layered interconnect structure to respective ones of the plurality of contact sites on the semiconductor chip as set forth in claim 87. In that regard, Peterson does not teach soldering a semiconductor chip to the mounting pads 103 or 104.

On page 14 of the answer, the examiner states:

> If Appellants had positively claimed the step of electrically connecting the semiconductor chip and circuitized substrate to the multi-layer structure, then a rejection under 35 U.S.C. 103(a) comprising Peterson in view of Frankeny (as

Prior Art of record), would have been made instead of the 35 U.S.C. 102(b) rejection.

In view of this statement, and claim 87 positively reciting both a semiconductor chip and the step of electrically connecting the semiconductor chip to the multi-layer interconnect structure it is unclear to us why the examiner maintained the anticipation rejection of claim 87.

In response to the appellants' argument that Peterson does not teach a semiconductor chip the examiner stated (answer, p. 11) that "In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963)." We do not agree. Under 35 U.S.C. § 103 all words in a claim must be considered in judging the patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). Furthermore, it is well established that the materials on which a process is carried out must be accorded weight in determining the obviousness of that process. See In re Pleuddemann, 910 F.2d 823, 825-28, 15 USPQ2d 1738, 1740-42 (Fed. Cir. 1990); In re Kuehl, 475 F.2d 658, 664-65, 177 USPQ 250, 255 (CCPA 1973); Ex parte Leonard, 187 USPQ 122, 124 (Bd. App. 1974). In our view, the case law clearly establishes that the position of the examiner with respect to claim 87 is in error.

For the reasons set forth above, the decision of the examiner to reject claim 87 under 35 U.S.C. § 102(b) is reversed.

Claims 80 and 91

Claims 80 and 91 are anticipated by Peterson for the reasons set forth in the answer. The appellants argue that Peterson does not teach:

(1) a thermally conductive layer having a selected thickness and coefficient of thermal expansion to substantially prevent failure of the solder connections as set forth in claims 80 and 91;

(2) a semiconductor chip as set forth in claims 80 and 91; and

(3) a second electrically conductive layer comprising a first plurality of shielded signal conductors as set forth in claim 91.

We find the appellants' argument unpersuasive for the following reasons.

First, Peterson's core section 102 is a thermally conductive layer having a selected thickness and coefficient of thermal expansion that will substantially prevent failure of the solder connections between the mounting pads and the surface-mounted devices. Peterson's core section 102 must have a thickness which is selected when the core section is made. Likewise, core section 102 must have a coefficient of thermal

expansion which is selected when the material for the core section is chosen. Thus, Peterson's core section 102 is a thermally conductive layer having a selected thickness and coefficient of thermal expansion. Additionally, since Peterson's object of his invention was to have a printed wiring board structure that possesses similar thermal expansion characteristics to the surface mount components to be attached (which reduces stress in the solder joints between the components and the printed wiring board), Peterson's core section 102 will substantially prevent failure of the solder connections between the mounting pads and the surface-mounted devices.

Second, while Peterson does not teach connecting a semiconductor chip to the mounting pads, claims 80 and 91 do not require such a connection. In that regard, claims 80 and 91 do not positively recite the semiconductor chip, instead claims 80 and 91 are drawn to a method of making a multi-layered interconnect structure **adapted for** electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections. Since the wiring board of Peterson has device mounting pads 103 and 104 for soldering surface-mount devices, the wiring board of Peterson is fully capable of having a semiconductor chip soldered thereto, which is all the claims 80 and 91 require with respect to the recitation of a semiconductor chip.

Third, Peterson clearly discloses a plurality signal conductors (the first conductive layer 105 on top of layer 102 in Figure 1 that is shielded by the second conductive layer 105 on top of layer 102 in Figure 1 and the conductive layer 102.

For the reasons set forth above, the decision of the examiner to reject claims 80 and 91 under 35 U.S.C. § 102(b) is affirmed.

Claims 82 to 86 and 93 to 97

In the brief (p. 6), the appellants have grouped claims 80 and 82 to 86 to stand or fall together and have grouped claims 91 and 93 to 97 to stand or fall together.

In accordance with the appellants grouping of claims and arguments provided, claims 82 to 86 fall with claim 80 and claims 93 to 97 fall with claim 91. Thus, it follows that the decision of the examiner to reject claims 82 to 86 and 93 to 97 under 35 U.S.C. § 102(b) is also affirmed.

The obviousness rejections

We will not sustain the rejection of dependent claims 88 to 90 under 35 U.S.C. § 103. As set forth above, all the limitations of parent claim 87 are not taught by Peterson. In the rejection of claims 88 to 90 under 35 U.S.C. § 103, the examiner did

not set forth any basis establishing that it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have modified Peterson so as to solder a semiconductor chip to the mounting pads 103 or 104. Accordingly, the examiner has not set forth a prima facie case of obviousness with respect to the subject matter of claims 88 to 90.

We will not sustain the rejection of claims 81 and 92. In the rejections of claims 81 and 92, the examiner stated (answer, p. 6) that:

> Peterson et al. disclose the step of laminating except for the specific range of temperature and pressure. At the time the invention was made it would have been obvious matter of design choice to one having ordinary skill in the art to specify a specific range of temperature and pressure in the step of lamination because Applicants have not disclosed that the specific temperature and pressure provide an advantage, are used for a particular purpose, or solve a stated problem. One ordinary skill in the art would have expected claimed inventions to perform equally well as Peterson et al's invention. Therefore, it would have been obvious matter of design choice to specify a specific range of temperature and pressure in the step of laminating the first and second dielectric layers onto the thermally conductive layer to obtain the invention as specified in claims 81 and 92.

The appellants argue (brief, p. 17) that the examiner has not supplied any evidence that the designer would choose a pressure of from about 1000 to about 1500 psi and a temperature of from about 600 to about 750° F as set forth in claims 81 and 92. We agree.

In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). A prima facie case of obviousness is established by presenting evidence that would have led one of ordinary skill in the art to combine the relevant teachings of the references to arrive at the claimed invention. See In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988) and In re Lintner, 458 F.2d 1013, 1016, 173 USPQ 560, 562 (CCPA 1972). Evidence of a suggestion, teaching, or motivation to modify a reference may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved, see Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630 (Fed. Cir. 1996), Para-Ordinance Mfg., Inc. v. SGS Importers Int'l., Inc., 73 F.3d 1085, 1088, 37 USPQ2d 1237, 1240 (Fed. Cir. 1995), cert. denied, 117 S. Ct. 80 (1996), although "the suggestion more often comes from the teachings of the pertinent references," In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998). The range of sources available, however, does not diminish the requirement for actual evidence. A broad conclusory statement regarding the obviousness of modifying a reference, standing alone, is not "evidence." See In re Lee, 277 F.3d 1338, 1342-45, 61 USPQ2d 1430, 1433-35 (Fed. Cir. 2002). See also In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). In this case, the examiner has not presented

evidence establishing that laminating at a pressure **and** temperature in the ranges recited in claims 81 and 92 would have been obvious at the time the invention was made to a person having ordinary skill in the art. Accordingly, the examiner has not set forth a prima facie case of obviousness with respect to claims 81 and 92.

For the reasons set forth above, the decision of the examiner to reject claims 81, 88 to 90 and 92 under 35 U.S.C. § 103 is reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 80, 82 to 87, 91 and 93 to 97 under 35 U.S.C. § 102(b) is affirmed with respect to claims 80, 82 to 86 and 91 to 97 and reversed with respect to claim 87; and the decision of the examiner to reject claims 81, 88 to 90 and 92 under 35 U.S.C. § 103 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JOHN P. McQUADE
Administrative Patent Judge

JEFFREY V. NASE
Administrative Patent Judge

JENNIFER D. BAHR
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